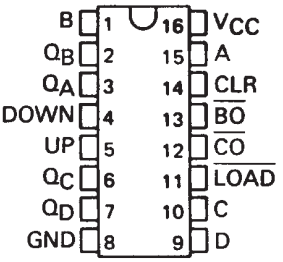
# SN54192, SN54193, SN54LS192, SN54LS193, SN74192, SN74193, SN74LS192, SN74LS193
# SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

SDLS074 – DECMEBER 1972 – REVISED MARCH 1988

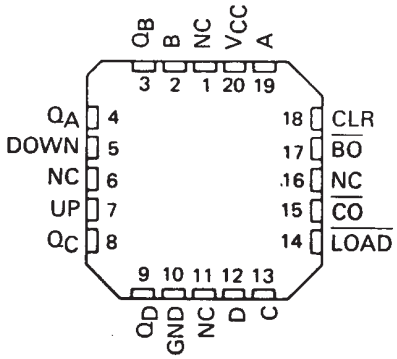
- **Cascading Circuitry Provided Internally**
- **Synchronous Operation**
- **Individual Preset to Each Flip-Flop**
- **Fully Independent Clear Input**

| TYPES | TYPICAL MAXIMUM COUNT FREQUENCY | TYPICAL POWER DISSIPATION |
|---|---|---|
| '192,'193 | 32 MHz | 325 mW |
| 'LS192,'LS193 | 32 MHz | 95 mW |

**SN54192, SN54193, SN54LS192, SN54LS193 . . . J OR W PACKAGE**
**SN74192, SN74193 . . . N PACKAGE**
**SN74LS192, SN74LS193 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54LS192, SN54LS193 . . . FK PACKAGE**
**(TOP VIEW)**




NC - No internal connection

## description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192 and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

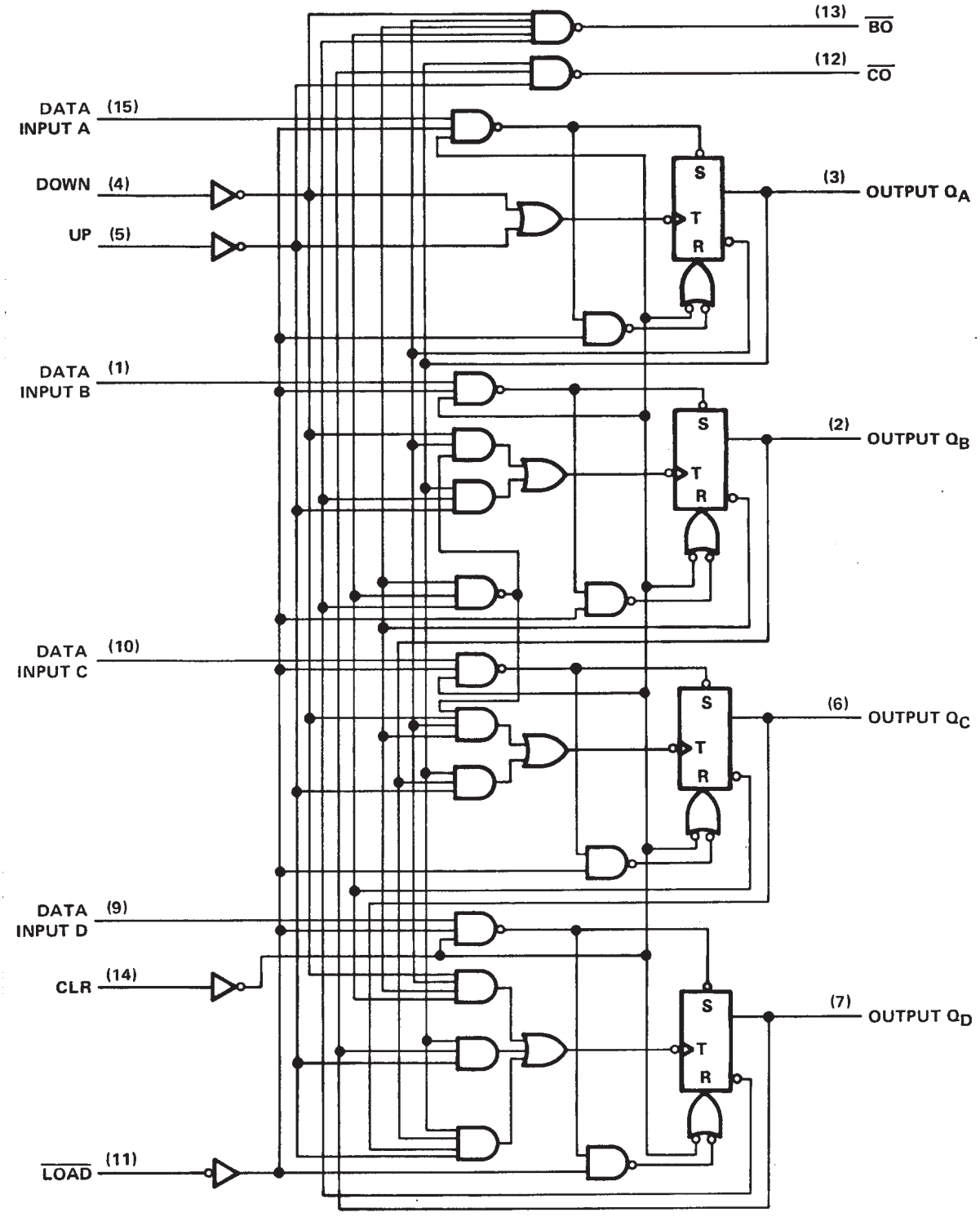
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | SN54' | SN54LS' | SN74' | SN74LS' | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 | 7 | 7 | 7 | V |
| Input voltage | 5.5 | 7 | 5.5 | 7 | V |
| Operating free-air temperature range | −55 to 125 | | 0 to 70 | | °C |
| Storage temperature range | −65 to 150 | | −65 to 150 | | °C |

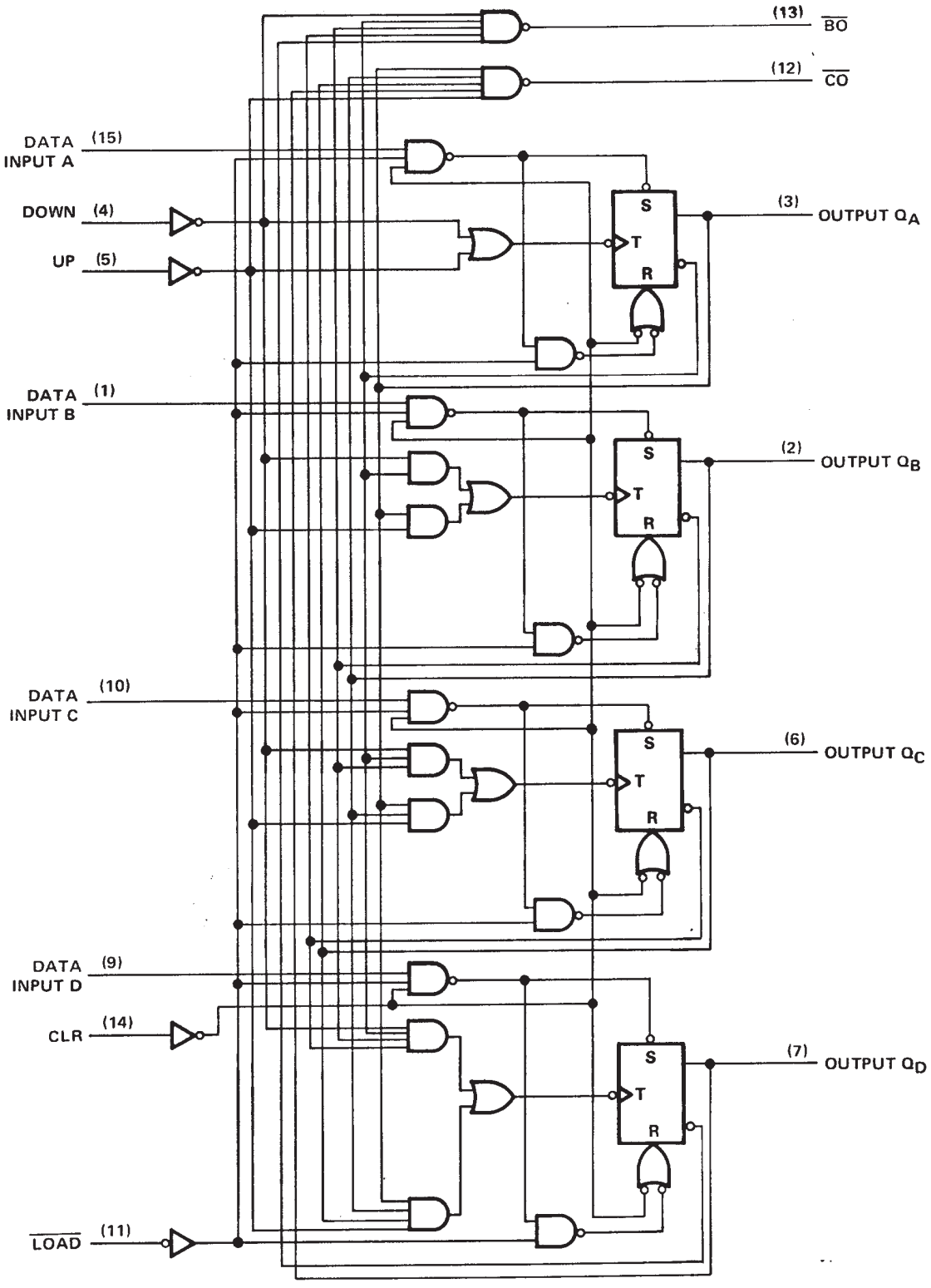
NOTE 1: Voltage values are with respect to network ground terminal.

## logic diagram (positive logic)



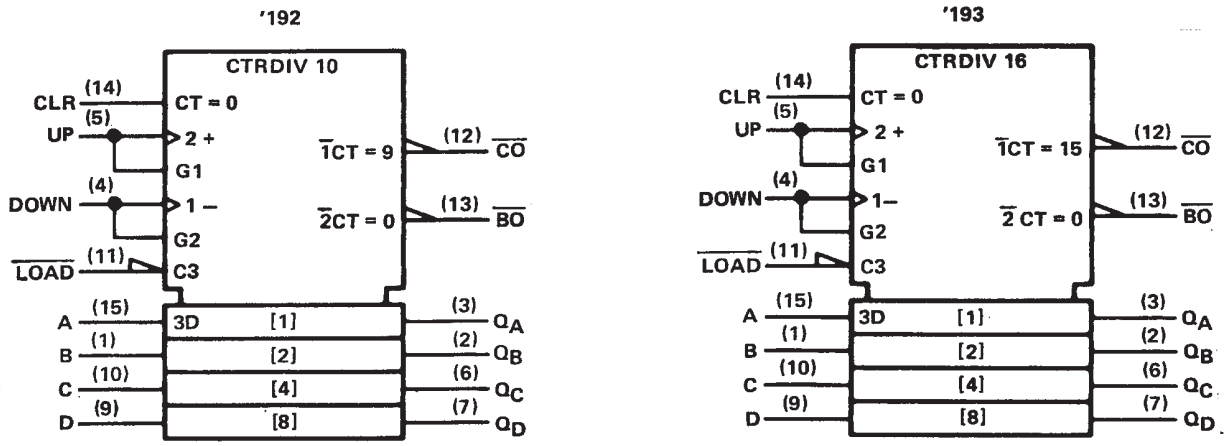

Pin numbers shown are for D, J, N, and W packages.

## logic diagram (positive logic)



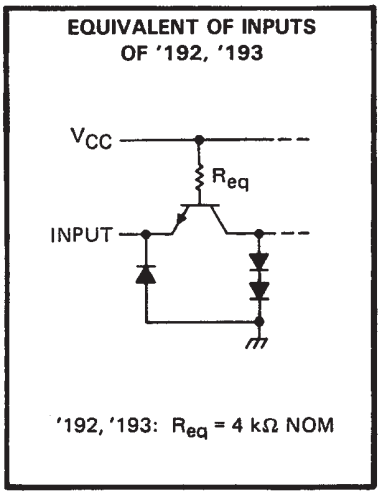

Pin numbers shown are for D, J, N, and W packages.

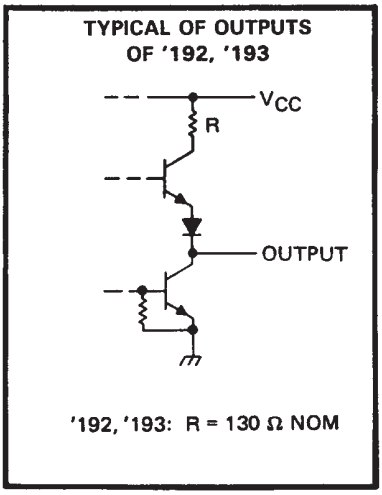
## logic symbols†

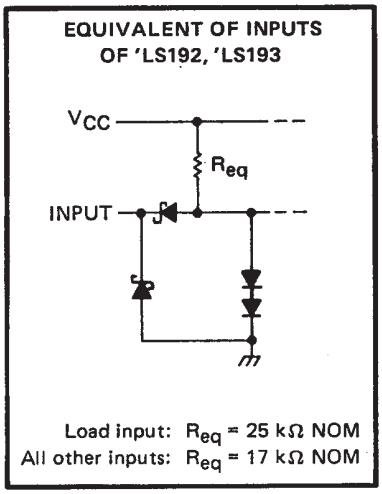


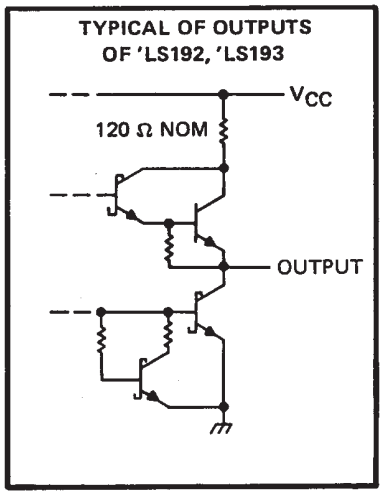

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

## schematics of inputs and outputs



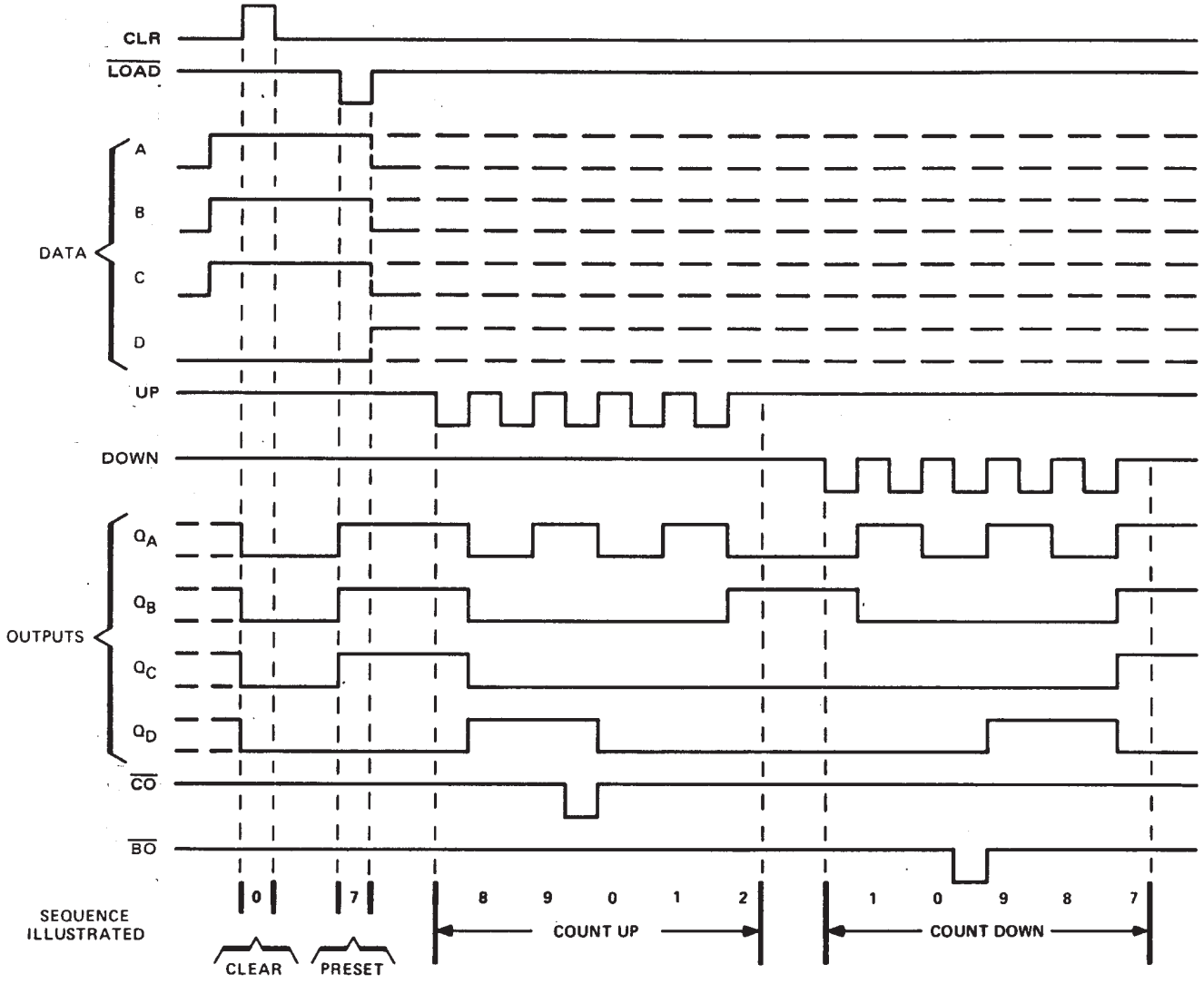



## '192, 'LS192 DECADE COUNTERS

### typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



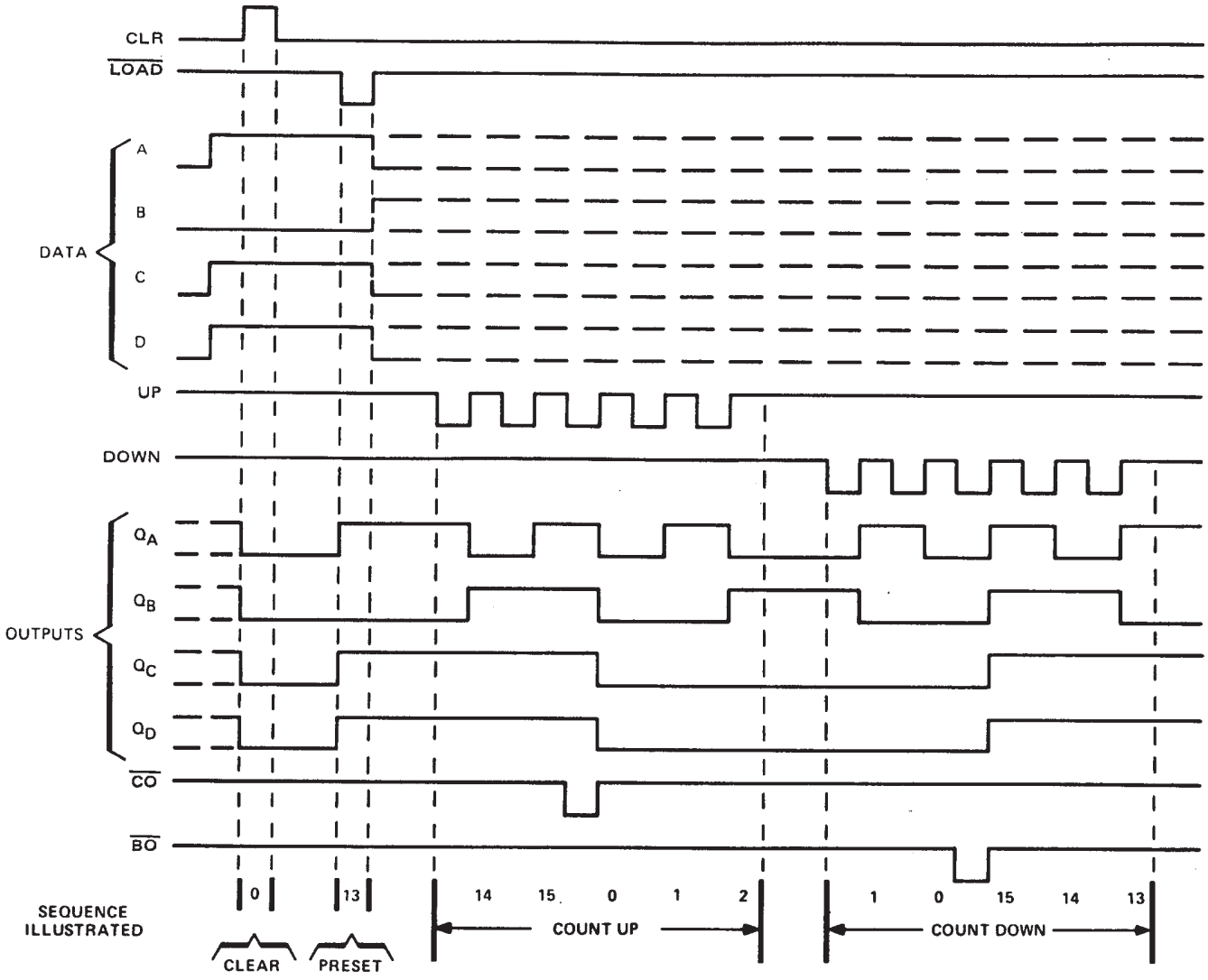

NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

## '193, 'LS193 BINARY COUNTERS

### typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.




NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

## recommended operating conditions

| | | | SN54192 SN54193 | | | SN74192 SN74193 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 25 | 0 | | 25 | MHz |
| $t_w$ | Width of any input pulse | | 20 | | | 20 | | | ns |
| $t_{su}$ | Data setup time, (see Figure 1) | | 20 | | | 20 | | | ns |
| $t_h$ | Hold time | Data, high or low | 0 | | | 0 | | | ns |
| | | $\overline{LOAD}$ | 3 | | | 3 | | | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54192 SN54193 | | | SN74192 SN74193 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −0.4 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | −20 | | −65 | −18 | | −65 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | 65 | 89 | | 65 | 102 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM INPUT | TO OUTPUT | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Figures 1 and 2 | 25 | 32 | | MHz |
| $t_{PLH}$ | UP | $\overline{CO}$ | | | 17 | 26 | ns |
| $t_{PHL}$ | | | | | 16 | 24 | |
| $t_{PLH}$ | DOWN | $\overline{BO}$ | | | 16 | 24 | ns |
| $t_{PHL}$ | | | | | 16 | 24 | |
| $t_{PLH}$ | UP OR DOWN | Q | | | 25 | 38 | ns |
| $t_{PHL}$ | | | | | 31 | 47 | |
| $t_{PLH}$ | $\overline{LOAD}$ | Q | | | 27 | 40 | ns |
| $t_{PHL}$ | | | | | 29 | 40 | |
| $t_{PHL}$ | CLR | Q | | | 22 | 35 | ns |

¶$f_{max}$ ≡ maximum clock frequency
$t_{PLH}$ ≡ propagation delay time, low-to-high-level output
$t_{PHL}$ ≡ propagation delay time, high-to-low-level output

## recommended operating conditions

| | | SN54LS192 SN54LS193 | | | SN74LS192 SN74LS193 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | | | −400 | | | −400 | μA |
| $I_{OL}$ | Low-level output current | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | 0 | | 25 | 0 | | 25 | MHz |
| $t_w$ | Width of any input pulse | 20 | | | 20 | | | ns |
| $t_{su}$ | Clear inactive-state setup time | 15 | | | 15 | | | ns |
| | Load inactive-state setup time | 15 | | | 15 | | | ns |
| | Data setup time (see Figure 1) | 20 | | | 20 | | | ns |
| $t_h$ | Data hold time | 5 | | | 5 | | | ns |
| $T_A$ | Operating free-air temperature range | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

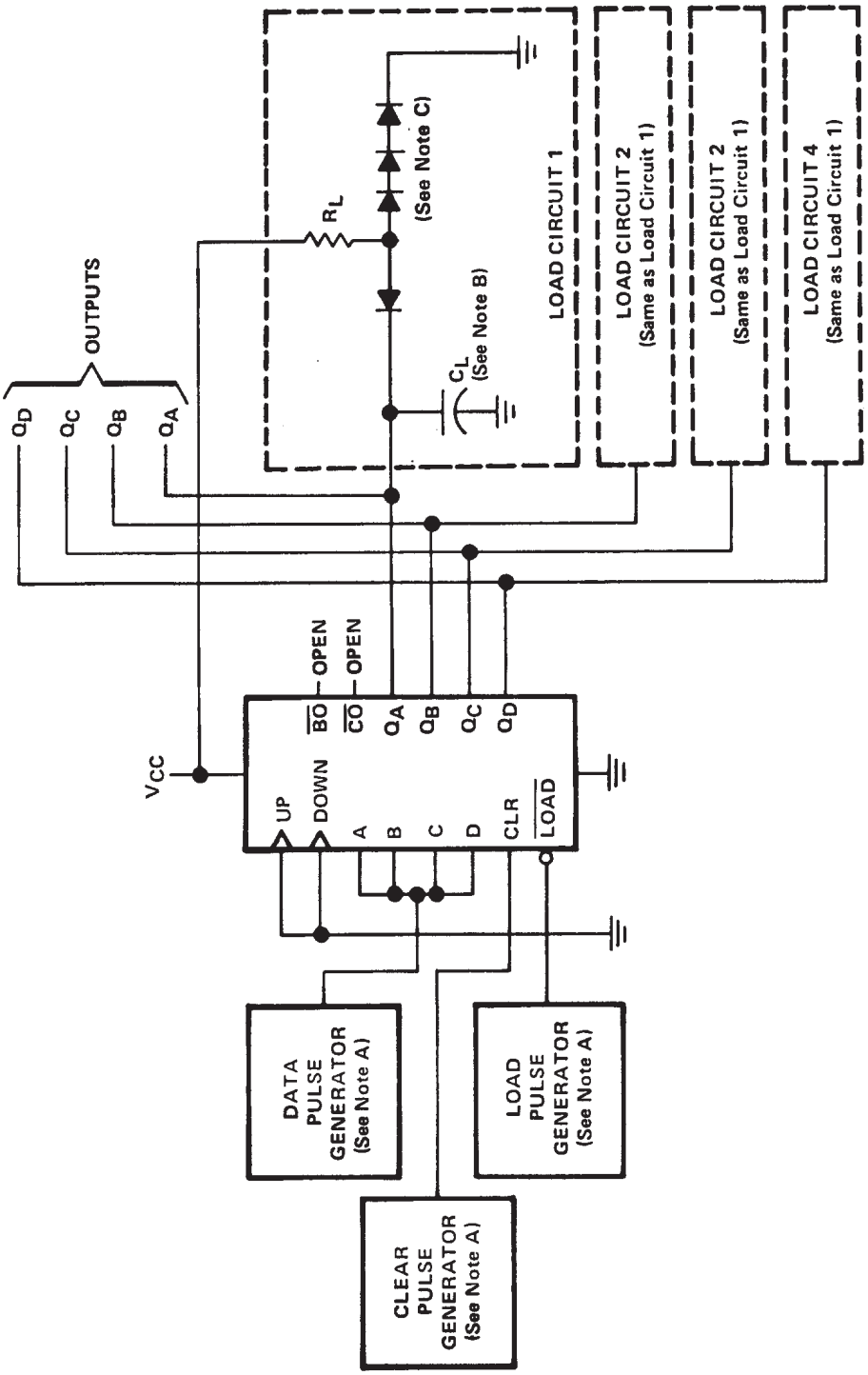
| PARAMETER | | TEST CONDITIONS† | | SN54LS192 SN54LS193 | | | SN74LS192 SN74LS193 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max, $I_{OH}$ = −400 μA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.15 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | | 19 | 34 | | 19 | 34 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: $I_{CC}$ is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | FROM INPUT | TO OUTPUT | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Figures 1 and 2 | 25 | 32 | | MHz |
| $t_{PLH}$ | UP | $\overline{CO}$ | | | 17 | 26 | ns |
| $t_{PHL}$ | | | | | 18 | 24 | |
| $t_{PLH}$ | DOWN | $\overline{BO}$ | | | 16 | 24 | ns |
| $t_{PHL}$ | | | | | 15 | 24 | |
| $t_{PLH}$ | UP OR DOWN | Q | | | 27 | 38 | ns |
| $t_{PHL}$ | | | | | 30 | 47 | |
| $t_{PLH}$ | $\overline{LOAD}$ | Q | | | 24 | 40 | ns |
| $t_{PHL}$ | | | | | 25 | 40 | |
| $t_{PHL}$ | CLR | Q | | | 23 | 35 | ns |

## PARAMETER MEASUREMENT INFORMATION




**TEST CIRCUIT**

**NOTES:** A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR $\leq$ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%

B. $C_L$ includes probe and jig capacitance.

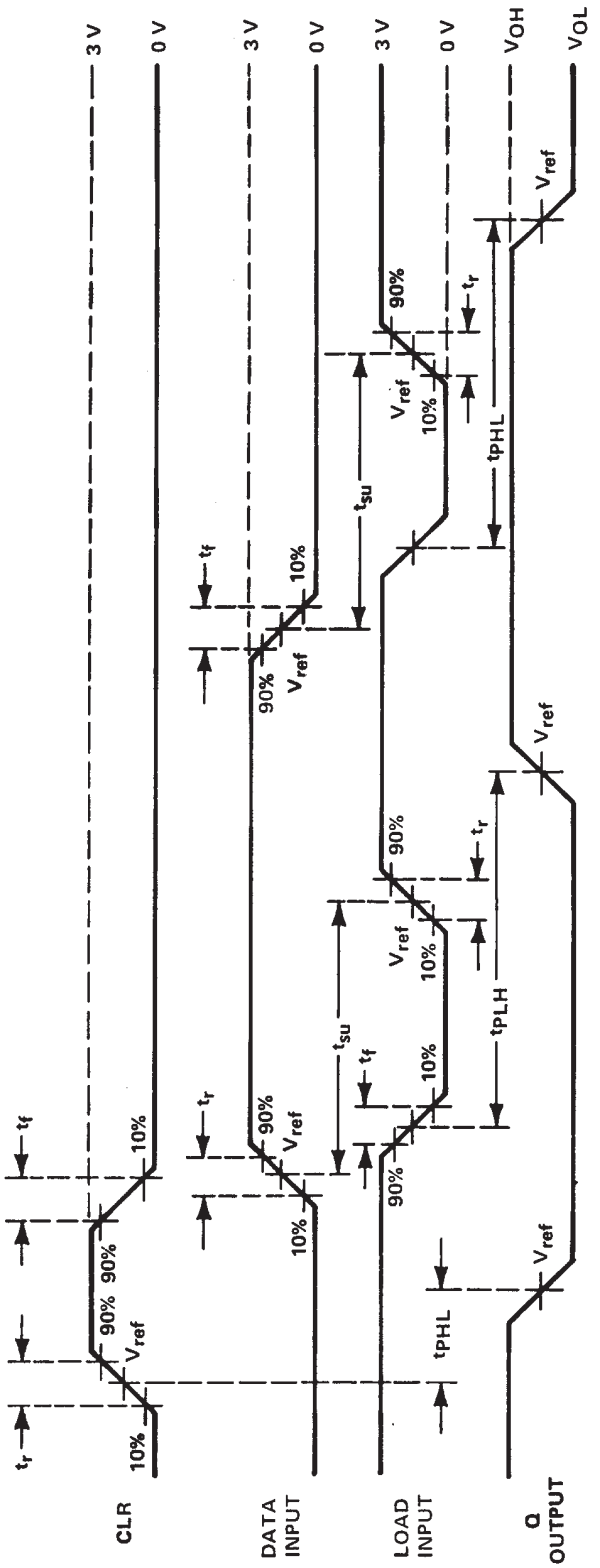
C. Diodes are 1N3064 or equivalent.

D. $t_r$ and $t_f \leq 7$ ns.

E. $V_{ref}$ is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

**FIGURE 1A – CLEAR, SETUP AND LOAD TIMES**

## PARAMETER MEASUREMENT INFORMATION

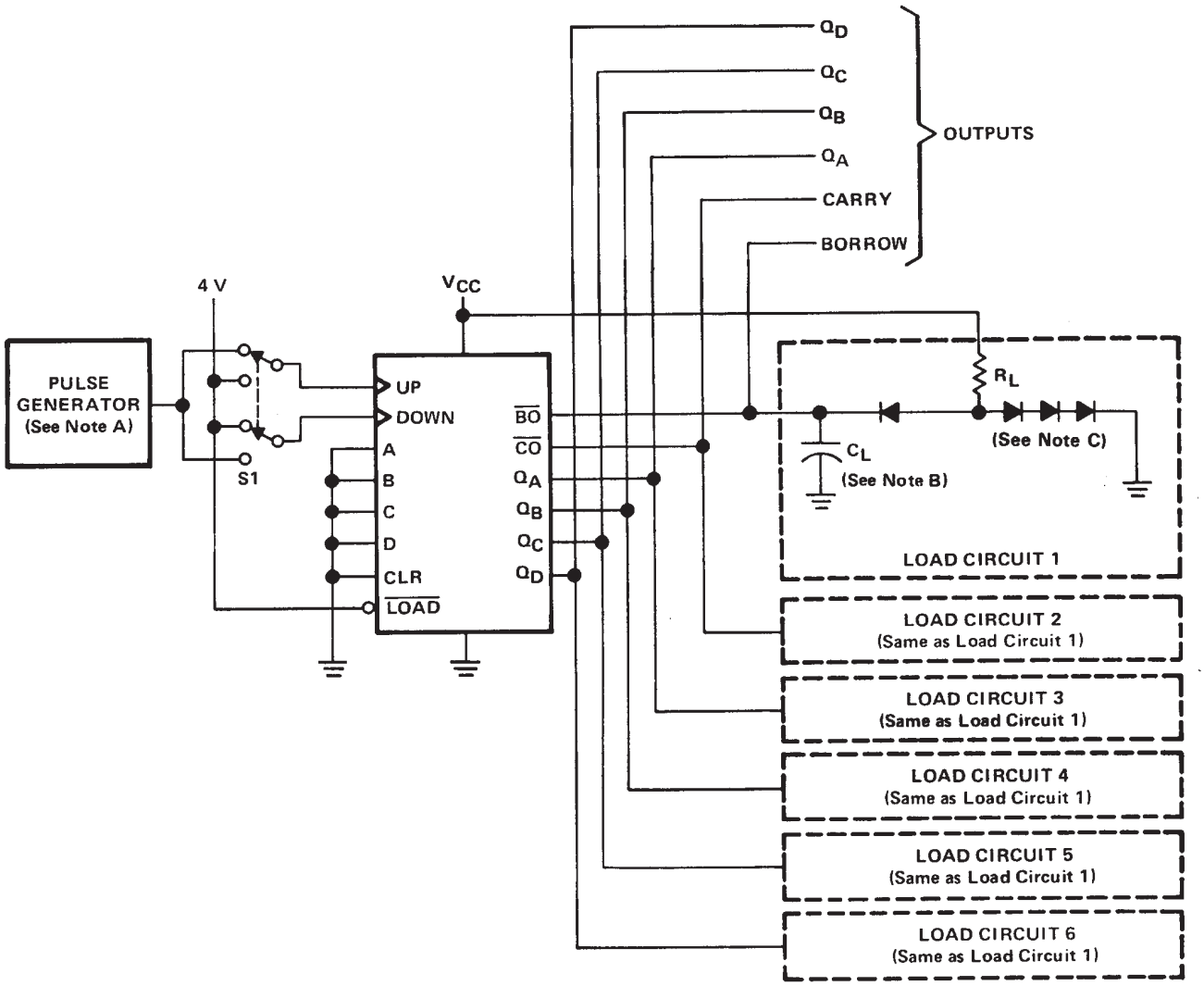



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%
B. $C_L$ includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. $t_r$ and $t_f \leq 7$ ns.
E. $V_{ref}$ is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

**FIGURE 1B – CLEAR, SETUP, AND LOAD TIMES**

## PARAMETER MEASUREMENT INFORMATION

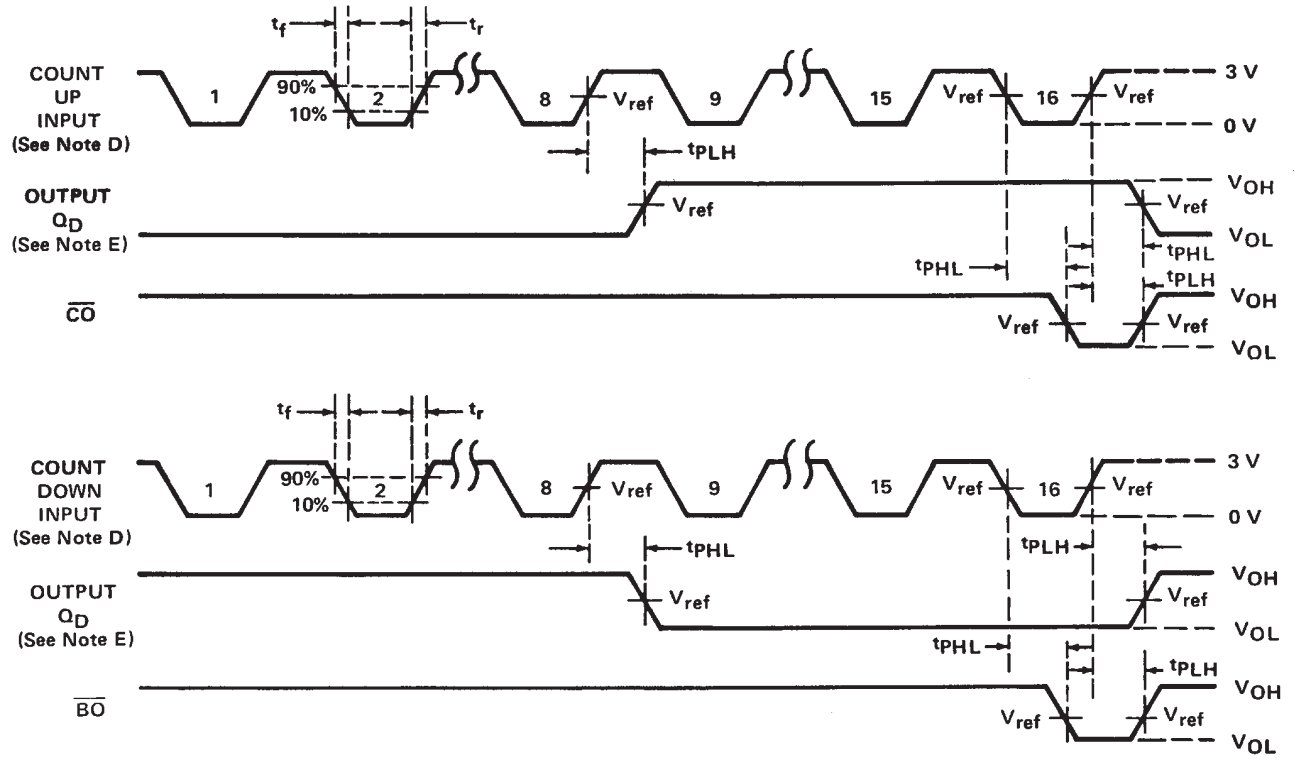



**TEST CIRCUIT**

NOTES: A. The pulse generators have the following characteristics: PRR ≈ 1 MHz, $Z_{out}$ ≈ 50 Ω, duty cycle = 50%.
B. $C_L$ includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Cout-up and dount-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs $Q_A$, $Q_B$, and $Q_C$ are omitted to simplify the drawing.
F. $t_r$ and $t_f$ ≤ 7 ns.
G. $V_{ref}$ is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

**FIGURE 2A – PROPAGATION DELAY TIMES**

## PARAMETER MEASUREMENT INFORMATION




VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: PRR ≈ 1 MHz, $Z_{out}$ ≈ 50 Ω, duty cycle = 50%.
B. $C_L$ includes probe and jig capacitance.
C. Diodes are 1N3064 or equivalent.
D. Cout-up and dount-down pulse shown are for the '193 and 'LS193 binary counters. Count cycle for '192 and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs $Q_A$, $Q_B$, and $Q_C$ are omitted to simplify the drawing.
F. $t_r$ and $t_f$ ≤ 7 ns.
G. $V_{ref}$ is 1.5 V for '192 and '193, 1.3 V for 'LS192 and 'LS193.

FIGURE 2B – PROPAGATION DELAY TIMES

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-9558401QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 5962-9558401QFA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 5962-9558401QFA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 76006012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 76006012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 7600601EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 7600601EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 7600601FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 7600601FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/01309BEA | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| JM38510/01309BEA | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| JM38510/31508B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508BFA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508BFA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508SEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508SEA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508SFA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| JM38510/31508SFA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN54192J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN54192J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN54193J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SN54193J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SN54LS193J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN54LS193J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SN74192N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74192N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74193N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74193N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74193N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74193N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74LS192D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| SN74LS192D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI |
| SN74LS192N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74LS192N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74LS193D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN74LS193DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| SN74LS193J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SN74LS193J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SN74LS193N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74LS193N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74LS193N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74LS193N3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI |
| SN74LS193NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74LS193NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74LS193NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS193NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS193NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS193NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54192J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54192J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54192W | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54192W | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54193J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SNJ54193J | OBSOLETE | CDIP | J | 16 | | TBD | Call TI | Call TI |
| SNJ54193W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI |
| SNJ54193W | OBSOLETE | CFP | W | 16 | | TBD | Call TI | Call TI |
| SNJ54LS193FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54LS193FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54LS193J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54LS193J | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54LS193W | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |
| SNJ54LS193W | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Level-NC-NC-NC |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

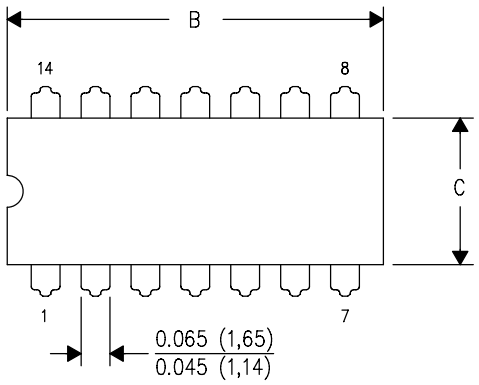
**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

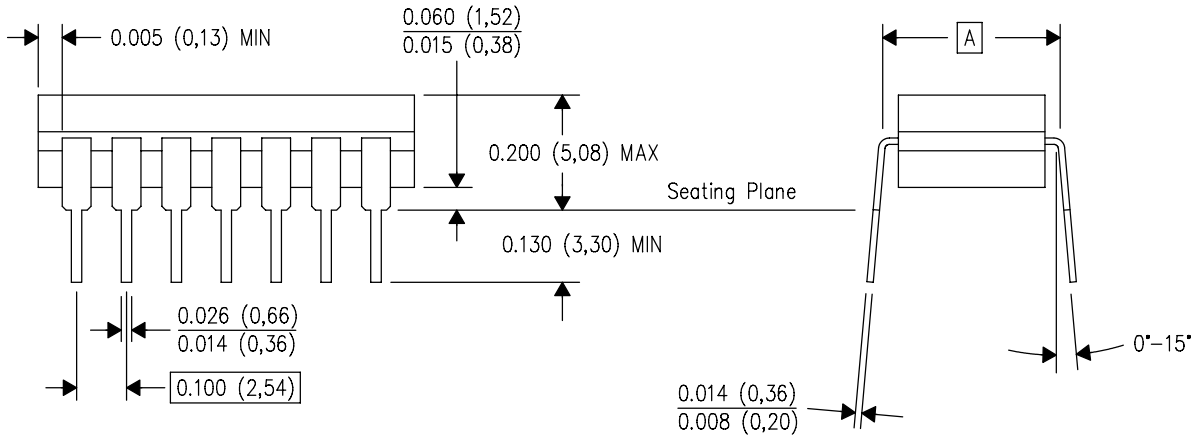
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



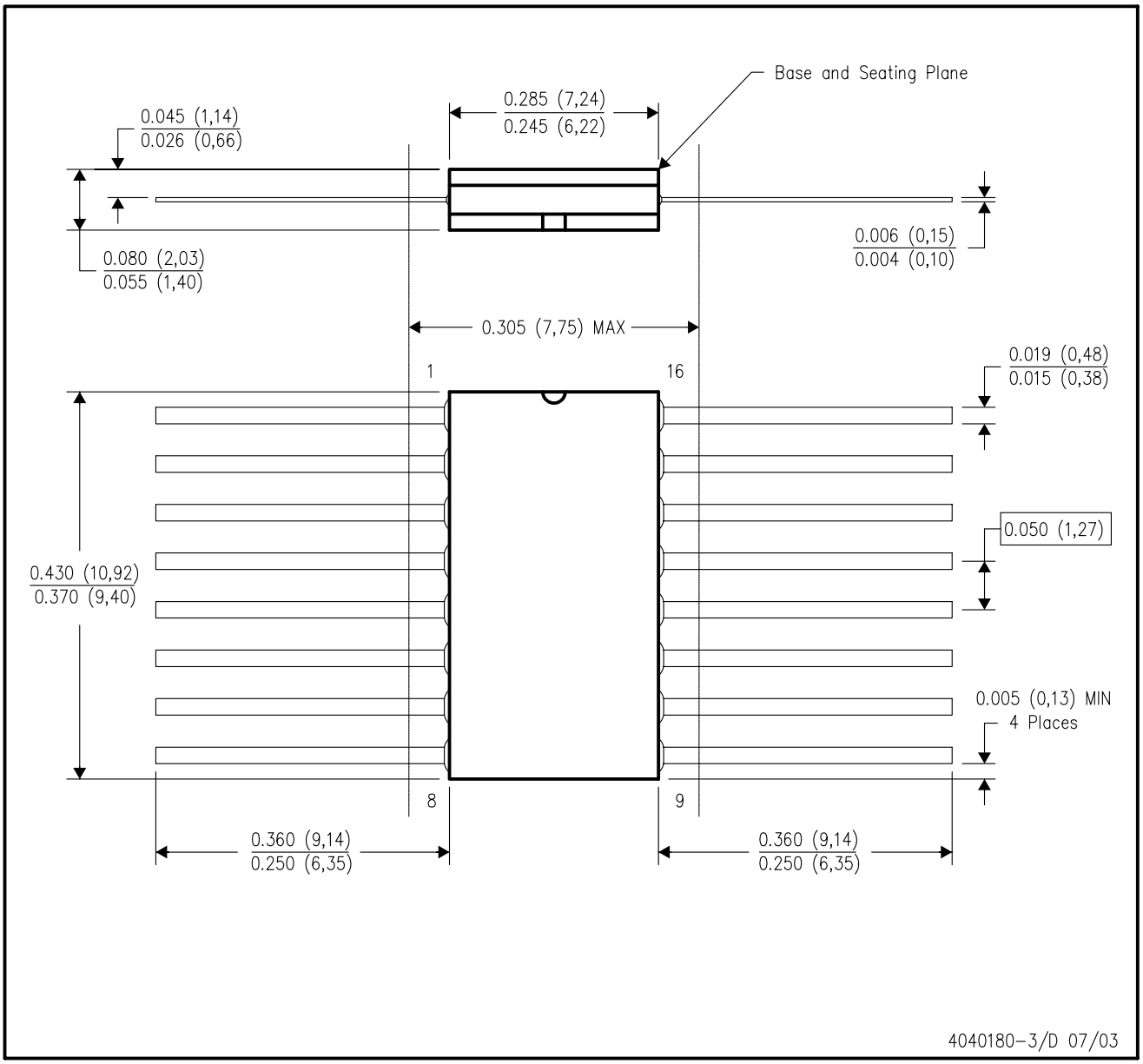

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

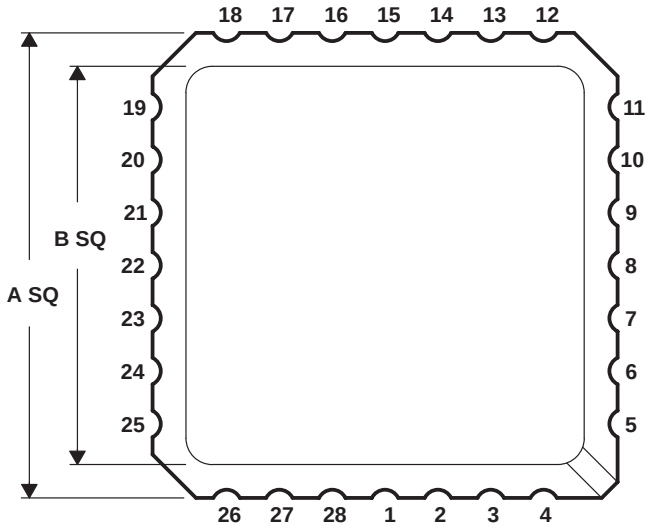
## W (R–GDFP–F16) CERAMIC DUAL FLATPACK



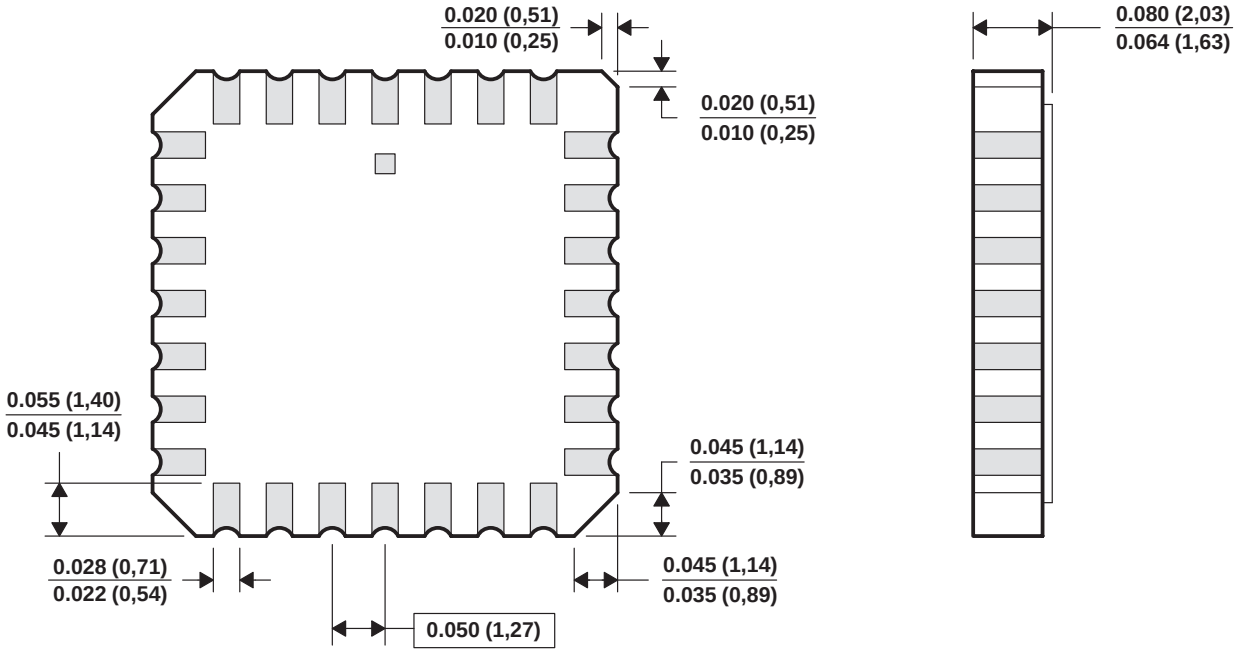

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



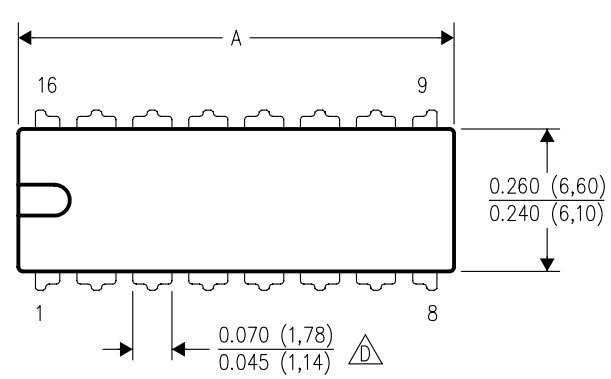

**4040140/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

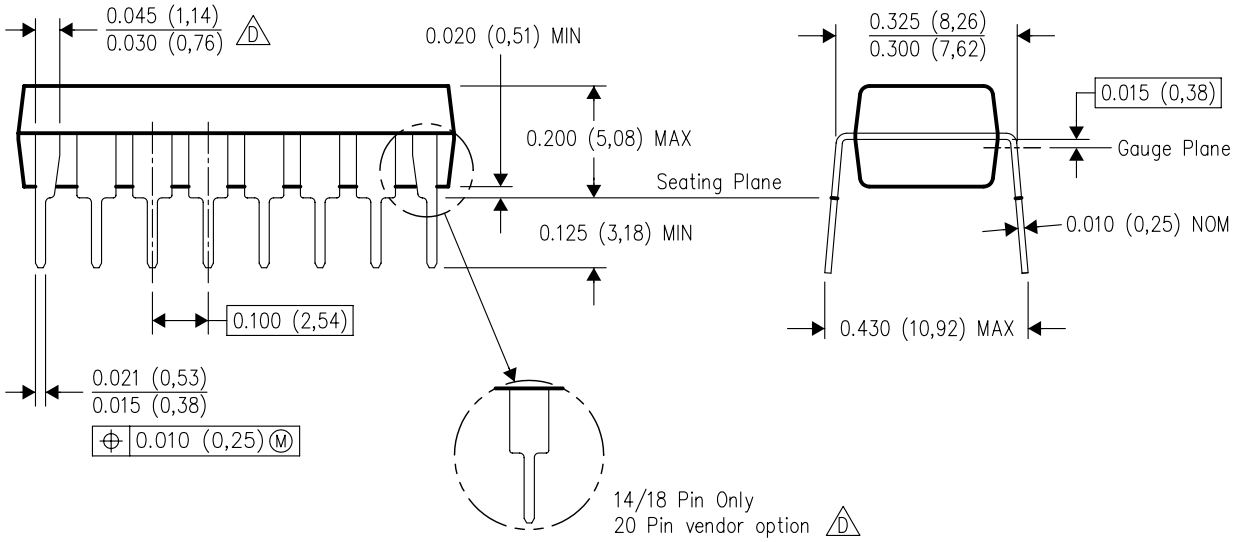
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



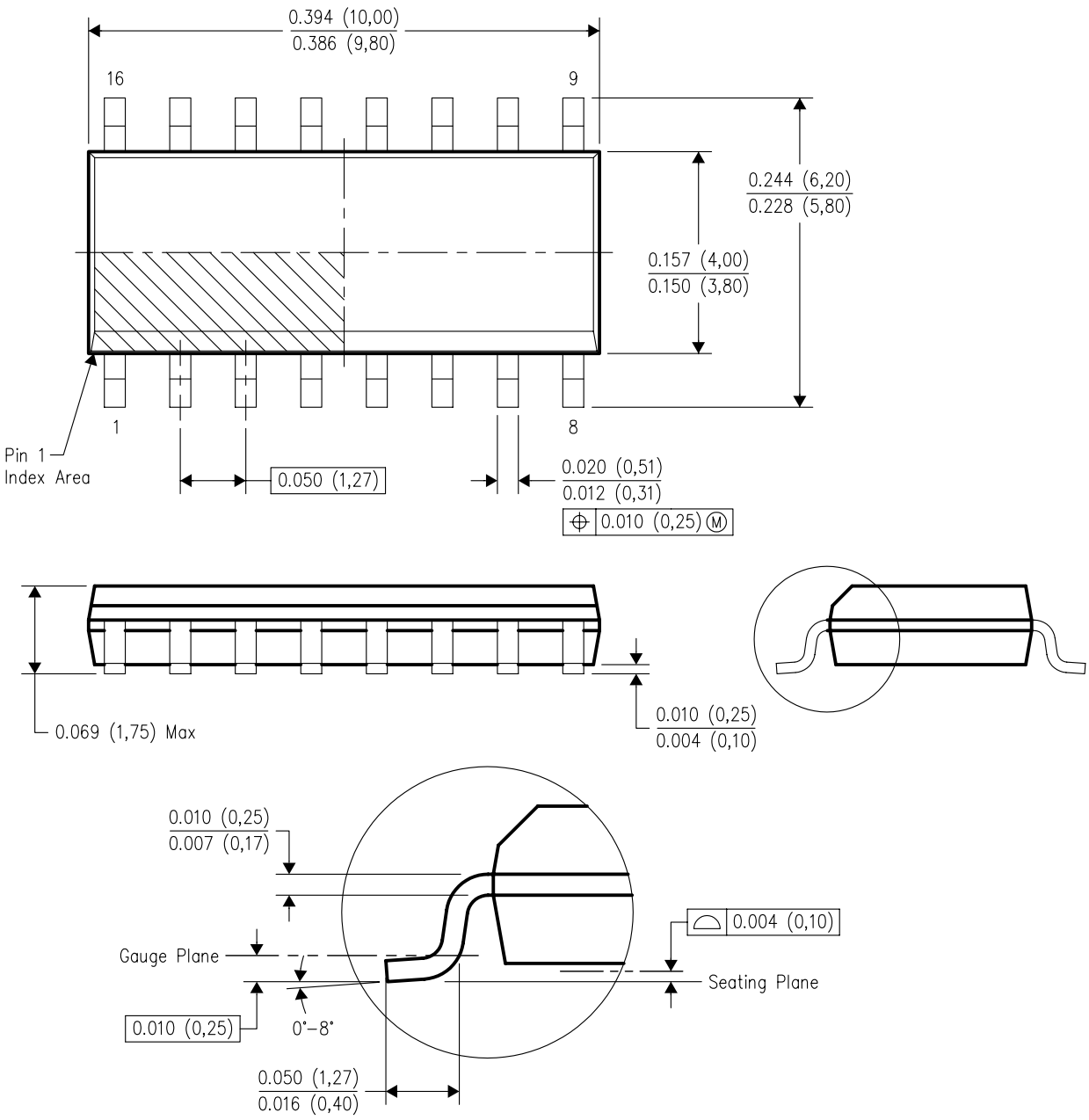

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

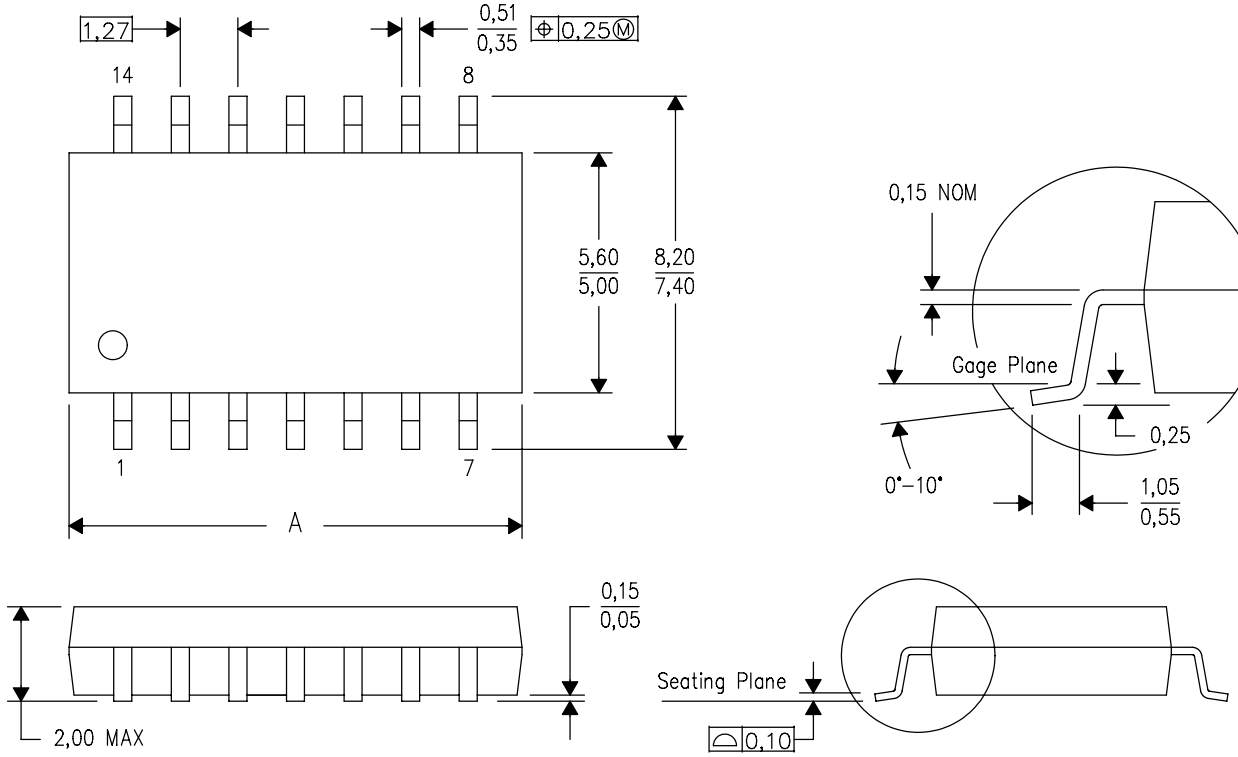



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265